

FFT Based VLSI Digital One Bit Electronic Warfare Receiver

By Henry C. Chien-In

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GOMACTech Government Microcircuit Applications and -

imple- menting a wideband electronic-warfare receiver Chien, M. Yajima, C based digital receiver has been designed for the

Abbreviations and Acronyms - Scribd -

Fleet Electronic Warfare Support Group Fast Fourier Transform First In Built-in-Test Pulse Compression Very Large Scale Integration Very Large

Self-assembled Molecular Templates: Microtubule- -

Self-assembled Molecular Templates: Microtubule-based Controlled Release for Biofouling Control and Medical Applications. Uploaded by Jonathan Selinger. 1 of 2:

Read Radar Signal Processing -

Readbag users suggest that Radar Signal Processing is worth less regular and structured than those of a digital filter or an FFT, 13.1 Electronic Warfare.

ISSUU - Military Embedded Systems January 2014 by -

Military Embedded Systems, January 2014, Embedded Signal Processing Enables Advanced Radars with low Latency, Fusing Sensor Data for Radar Displays, Radar

www.ebscohost.com -

Military art and science--Technological innovations.,Military engineering.,Warfare, Very large scale integration electronic systems.,Digital

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electronic systems 079. Electronic Warfare 109, 148, Light-Based Digital Network 122. receiver demodulator 271.

dblp.dagstuhl.de -

Aleksandra Mojsilovic: A logistic regression model for small sample classification problems with hidden variables and non-linear relationships: an application in

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2.1.2 Electronic Warfare Systems. . 1. FIR digital filters the Fast Fourier Transform has many algorithmic realizations.

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VLSI Implementation of Split-Radix Fast Fourier -

VLSI Implementation of Split-Radix Fast Fourier Transform: A Survey - Free download as PDF File (.pdf), IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)

IEEE Xplore - Conference Table of Contents -

ASIC Conference and Exhibit, 1993. Proceedings., Chien-In In Henry A specialized ASIC signal processor has been developed for electronic warfare

IEEE Xplore Abstract - Low cost VLSI design of a -

a low-cost VLSI implementation of a (N-1) memory words to get the FFT where flexible large size FFT processor is needed such as digital video

IEEE Xplore Abstract - FFT based VLSI digital -

Some details are presented of a VLSI (1.2- μ m CMOS) digital array signal processor (DASP) which has been designed for applications in high-performance fast Fourier

01 Erbium-Doped Fiber -

10 DESIGN AND ANALYSIS OF PROPOSITIONAL-LOGIC RULE-BASED SYSTEMS. 10.1 Real (FFT) and other digital How can you use the fast Fourier transform

platinum.ohiolink.edu -

netlib-retain.dat ocm49851636 Quick arithmetic a self-teaching guide / Robert A. Carman, Marilyn J. Carman. ocm48138818 Entrepreneurial marketing lessons from Wharton

ANALYSIS AND DESIGN OF DIGITAL RECEIVER USING -

ANALYSIS AND DESIGN OF DIGITAL RECEIVER USING MULTI-BIT FFT ALGORITHM
Indian Streams Research Journal C. Montgomery, B.Y. Tsui, David Pok, Chien In Henry Chen

Interval Based X-Masking for Scan Compression -

Chien-In Henry Chen: Pages: 143-147 Based on the exact solution of the 1-D for digital and analog design with CNFET. Based on the

Efficient memory partitioning for parallel data -

ACM Transactions on Design Automation of Electronic It is based on extracting a unique bit-level polynomial function and Fast Fourier Transform

/tardir/mig/a348449 - Defense Technical -

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ABSTRACT A design for the monobit receiver application specific integrated circuit (ASIC) will

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VLSI IMPLEMENTATION OF PIPELINED FFT BASED ON SDC-SDF pipelined fast Fourier transform architecture, ISRASE eXplore Digital Library Fig.1: